VEL TECH HIGH TECH

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An Autonomous Institution

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COURSEDETAILS

FACULTYNAME	:	C.D.MERLIN	**FACULTYCODE**	:	HTS1630
COURSENAME	:	DIGITAL LOGIC CIRCUITS	**COURSECODE**	:	21HE32T
YEAR/SEM/ DEPT	:	II YR/III SEM/CSE – AIML	**ACADEMICYEAR**	:	2023-2024 (ODDSEM)

OBJECTIVES

- To Simplify logic digital Circuits using Boolean Functions.

C302.1: ***Simplify*** logic functions using Boolean Algebra and K-map.

SYLLABUS

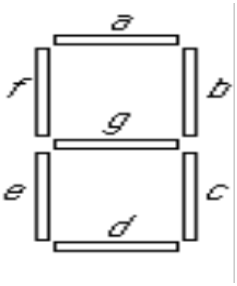
UNIT I BOOLEAN ALGEBRA AND LOGIC GATES

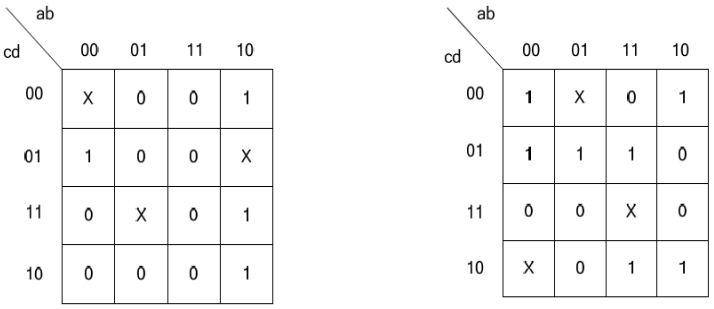
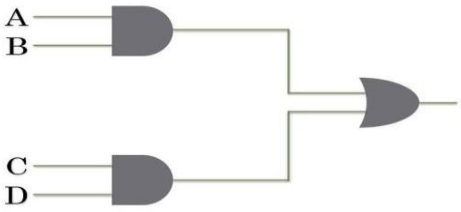
Number Systems – Arithmetic Operations – Binary Codes- Tabulation method – Theorems and Properties of Boolean Algebra – Boolean Functions – Canonical and Standard Forms – Simplification of Boolean Functions using Karnaugh Map – Logic Gates – Universal gates Implementations.

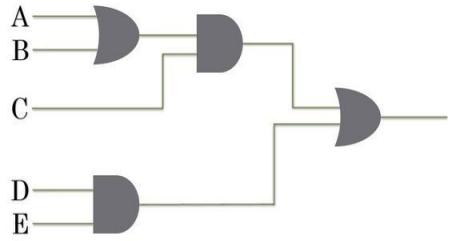
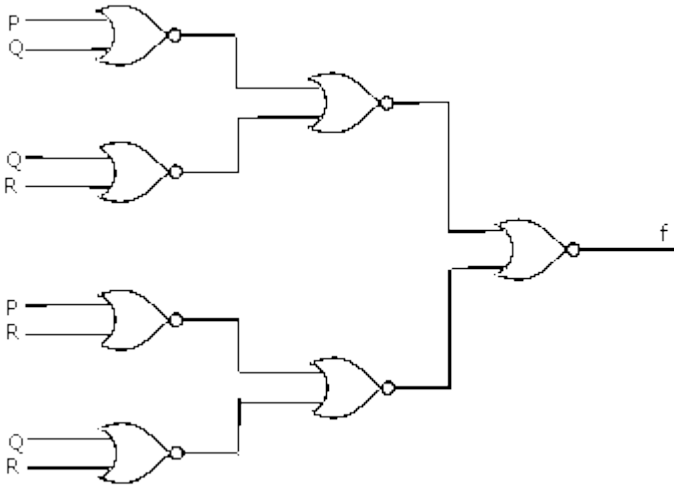
UNIT II COMBINATIONAL LOGIC CIRCUITS

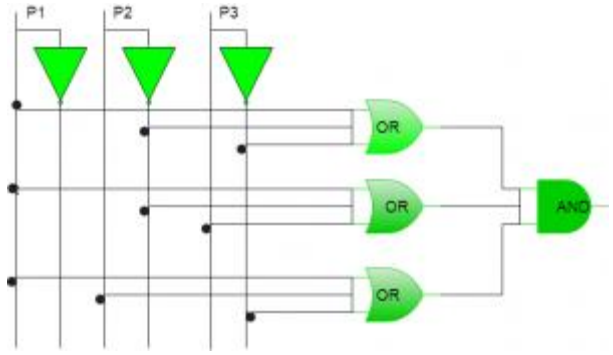
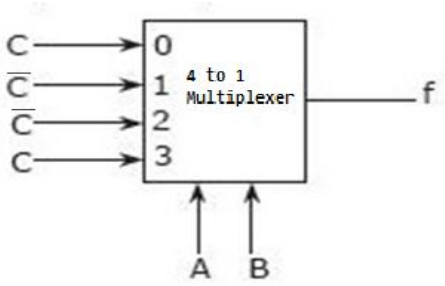
Combinational Circuits – Analysis and Design Procedures – Adder-Subtractor -Multiplier – Decoders – Encoders – Multiplexers –Demultiplexers-Implementation of combinational circuits using mux, demux, encoder, decoder-Introduction to VHDL – VHDL Models of Combinational Circuits-Case study (Calender subsystem).

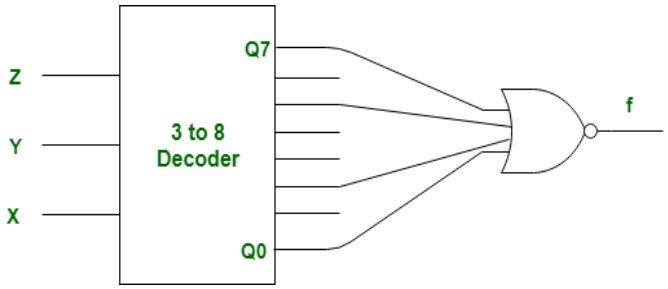
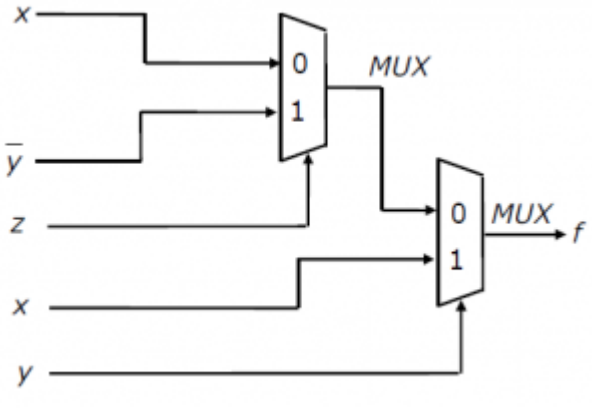
Batch No.	Assignment Problems	CO Relevance	Knowledge Level
1	(A)Snerdley's Automated Cafeteria orders a machine to dispense coffee, tea, and milk. Design the machine so that it has a button (input line) for each choice and so that a customer can have *at most one* of the three choices. Diagram the circuit to insure that the "at most one" condition is met. (B)Implement EX-OR gate using only NAND gates (C) Design a logic circuit to simulate the function f(A,B,C)=A(B+C) by using only NAND gates. *Introduction *Truth table *Logic gate Representation *Solution *Conclusion *References	CO1	K4
2	The nation of Upper Slobovia has gained a missile defense capability governed by its Security Council. The Council consists of four members:the U.S. (Upper Slobovian) President and three Counselors (theChiefs of Staff of the Army and Air Force plus the President's UncleHomer). The missile system is to be activated by a device obeying these rules: (A)each member of the Security Council has a button to push;	CO1	K4

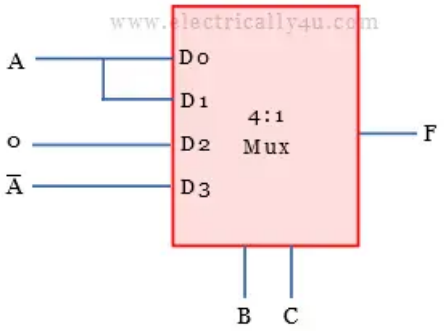
	(B) the missiles fire only if the President and at least one Counselor push their buttons. (C) Design the rocket firing circuitry. *Introduction *Truth table *Logic gate Representation *Solution *Conclusion *References		
3	Most calculators, digital clocks, and watches use the "seven segment display" format. In this setup, as the diagram shows, there are seven segments that can be lit in different combinations to form the numerals 0 through 9. For example,"1" is formed by lighting segments *b* and *c*; "2" consists of segments *a*, *b*, *g*, *e*, and *d*. "4" is composed of segments *b*, *c*,*f*, and *g*.  (A)Design circuitry to run a seven-segment display for one digit. The input consists of a four-bit digit (where each bit is an input line). The outputs are *a*, *b*, *c*, *d*, *e*, *f*, and *g* of the seven segment diagram (1 = light the segment, 0 = do not light the segment). (B)From a truth table, write and simplify *seven* Boolean expressions. (C) Draw the seven minimal circuits. Note: There are only *ten* rows of input in the table corresponding tothe digits 0 (0000_{two} through 9 (1001_{two}). *Introduction *Truth table *Logic gate Representation *Solution *Conclusion *References	CO1	K4
4	(A)A circuit outputs a digit in the form of 4 bits. 0 is represented by 0000, 1 by 0001, ..., 9 by 1001. A combinational circuit is to be designed which takes these 4 bits as input and outputs 1 if the digit ≥ 5, and 0 otherwise. If only AND, OR and NOT gates may be used, what is the minimum number of gates required? (B)Use DeMorgan's Theorems to simplify the following expressions: $\overline{\overline{a+d}\cdot\overline{b+\overline{c}}\cdot\overline{\overline{c}+d}}$ (C) Solve $\overline{x}+y\overline{x}=\overline{x}(1+y)=\overline{x}$	CO1	K4

	*Introduction *Truth table *Logic gate Representation *Solution *Conclusion *References		
5	Karnaugh Maps are useful for finding minimal implementations of Boolean expressions with only a few variables. However, they can be a little tricky when "don't cares" (X) are involved. Using the following K-Maps:  i) Find the minimal sum of products expression. ii) Find the minimal product of sums expression. iii) Are your solutions unique? If not, list and show the other minimal expressions. *Introduction *Steps involved *Solution *Conclusion *References	CO1	K4
6	(A)Implement the Same Boolean Function with NAND only in the following Circuit  (B)Illustrate the range of values that can be represented using n-bit 2's complement form of representation with an example? What is the corresponding range with n-bit 1's complement form? (C) Write the applications of Gray code *Introduction*Explanation*Solution*Conclusion *References	CO1	K4
7	(A) Implement the Same Boolean Function with NAND only in the following Circuit	CO1	K4

	 (B)Convert hexadecimal B2.A1 to Octal equivalent. (C) Convert Boolean expression in standard form F=y'+xz'+xyz *Introduction*Explanation*Solution*Conclusion*References		
8	(A)What is the Boolean expression for the output f of the Combinational logic circuit of NOR gates given below?  (B)Express the Boolean function F = A + B'C as standard sum of minterms. (C) Express the Boolean function F = xy + x'z as a product of maxterms *Introduction*Explanation*Solution*Conclusion*References	CO1	K4
9	(A) Find the output of the following combinational circuit.	CO1	K4

	 (B)Select the gate which produces a high output signal only when both inputs are low and explain how it can be used in in a real-time fire and smoke detection to alert occupants of a building. (C)Design a logic circuit that has three inputs A,B,C whose output will be high only when a majority of the inputs are high. *Introduction*Explanation*Solution*Conclusion*References		
10	(A)Explain how logic circuit that takes a binary input and produces an output that corresponds to a specific output line can be used in laptop. (B)How can the concept of universal gates be applied in the field of neural networks or artificial intelligence? Explore the potential benefits and challenges of using universal gates in these domains. (C) Design a gray to binary code converter. *Introduction*Explanation*Solution*Conclusion*References	CO1	K4
11	(A)Design a **binary adder** that adds three two-bit numbers. The six inputs are the bits of the three numbers to be added. The four outputs are the bits of the sum. Draw a separate circuit for each bit of the sum. (B)Consider the circuit in below figure. Find *f*  (C) If half adders and full adders are implemented using gates, then for the addition of two 17 bit numbers (using minimum gates) How many number of half adders and full adders will be required? *Introduction*Explanation*Solution*Conclusion*References	CO2	K4

12	(A)What Boolean function does the circuit below realize ?  (B)Design a **binary multiplier** that multiplies two two-bit numbers. The four inputs arethe bits of the two numbers to be multiplied. The four outputs are the bits of theproduct. Draw a separate circuit for each bit of the product. (C)Use DeMorgan's Theorems to simplify the following expressions: $\overline{\overline{(a \cdot b \cdot \overline{c})} + \overline{(\overline{c} \cdot d)}}$ *Introduction*Explanation*Solution*Conclusion*References	CO2	K4
13	(A) Consider the following circuit. What represents f (x, y, z)?  (B)Use DeMorgan's Theorems to simplify the following expressions: $\overline{\overline{(a + d)} \cdot \overline{(\overline{b} + c)}}$ (C) Implement a two-input AND gate using two 2-1 multiplexers. *Introduction*Explanation*Solution*Conclusion*References	CO2	K4
14	(A)Design a **two-bit binary adder**. For example, 10 + 11 = 101. The truth table should contain four input columns for the bits of the numbers to be added and three output columns, one for each bit of the sum. Draw a separate circuit for each bit of the sum. (B)Implementation of Half Adder using NAND gates (C)Subtract 748 from 983 using 9's complement method	CO2	K4

	*Introduction*Explanation*Solution*Conclusion*References		
15	(A)For the given multiplexer circuit, determine the logic function.  (B) Implement the boolean expression F(A, B, C) = ∑ m(0, 2, 5, 6) using 4 : 1 multiplexer. (C)Implementation of Half Subtractor using NAND gates *Introduction*Explanation*Solution*Conclusion*References	CO2	K4
16	(A)Implement a 3-to-8 line decoder using a 2-to-4 line decoder and a 3-input AND gate. (B)Design a 16-channel analog multiplexer using a combination of digital multiplexers and demultiplexers. Implement this design using a VHDL model and test its functionality by simulating various input scenarios. (C)Implementation of Half Subtractor using NOR gates *Introduction*Explanation*Solution*Conclusion*References	CO2	K4
17	(A)Design a VHDL model for a 4-to-1 multiplexer using only basic logic gates (AND, OR, NOT). Test the design using suitable test vectors. (B) Implement a VHDL model for a BCD (Binary Coded Decimal) to 7-segment display decoder. Verify the correctness of the decoder by providing different BCD inputs and observing the corresponding 7-segment outputs. (C)Implementation of Half Adder using NOR gates *Introduction*Explanation*Solution*Conclusion*References	CO2	K4
18	(A)How can adder and subtractor circuits be integrated into larger systems or architectures, such as CPUs or digital signal processors? Discuss the interactions, dependencies, and optimizations that can be employed for seamless integration. (B) Can we design an adder circuit that operates on non-binary inputs, such as fractional or decimal numbers? Discuss the challenges and potential	CO2	K4

	applications of such a design. (C)Implement BCD to 7 Segment Decoder *Introduction*Explanation*Solution*Conclusion*References		
19	(A) How can multiplier circuits be adapted or optimized for specific applications, such as digital filters, image processing, or cryptography? Discuss the requirements and considerations for designing multipliers in specialized domains. (B) How can we optimize MUX circuits to achieve faster switching times and higher data throughput? Explore novel techniques, architectures, or materials that can improve the performance of MUX. (C) Implement the boolean expression F(A, B, C) = ∑ m(2, 3, 6, 7) using a multiplexer. *Introduction*Explanation*Solution*Conclusion*References	CO2	K4
20	(A) Design the conversion circuit that convert BCD code to excess-3 code? (B) Design a combinational circuit that generates 9's complement of a 3 input numbers and implementing it using 3 gates only. (C) Explain the procedure of designing the combinational circuits. *Introduction*Explanation*Solution*Conclusion*References	CO2	K4

REFERENCES

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